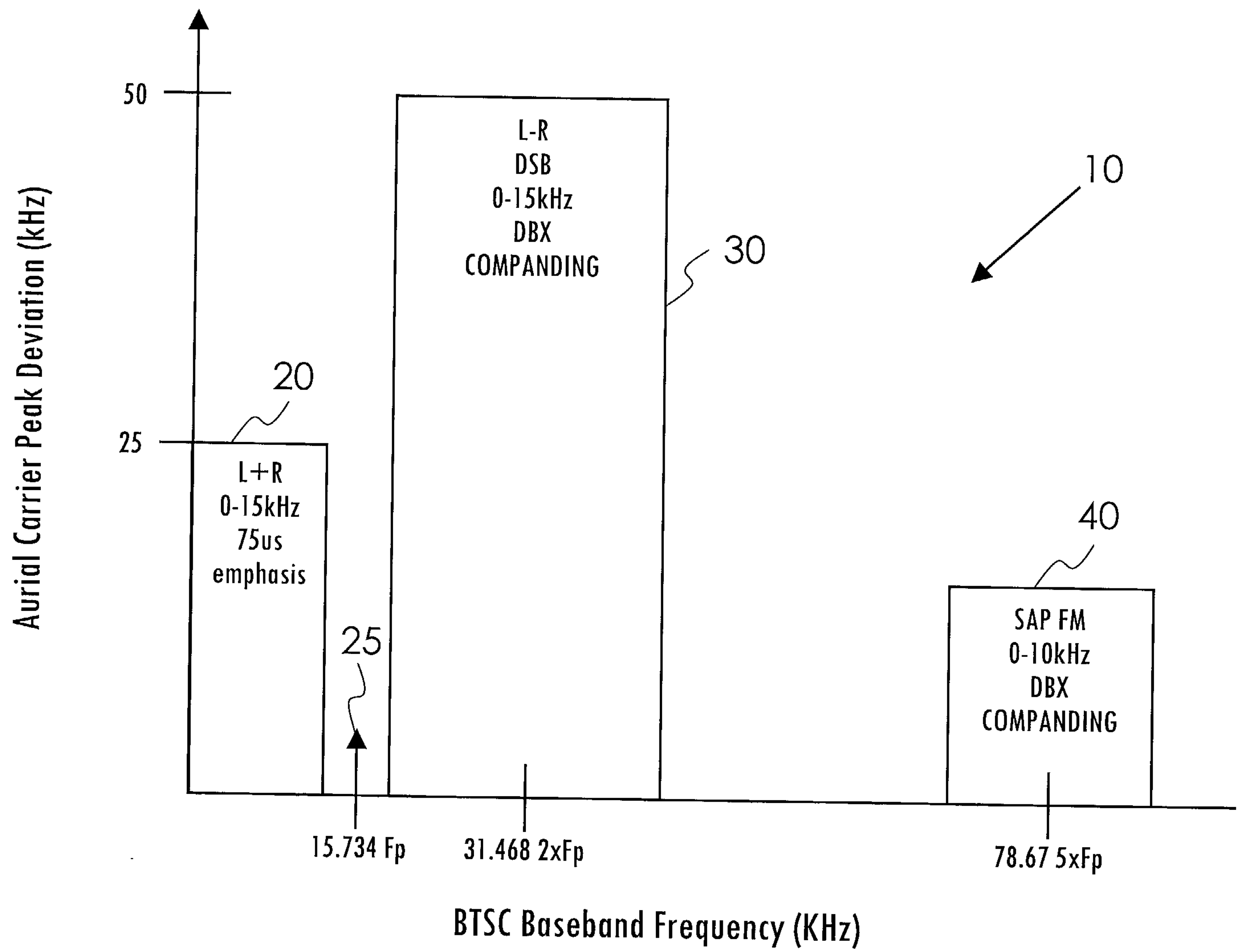
Aurial Carrier Peak Deviation (kHz)
50
25
L+R
0-15kHz
75us
emphasis
20
25
L-R
DSB
0-15kHz
DBX
COMPANDING
30
10
SAP FM
0-10kHz
DBX
COMPANDING
40
15.734 Fp
31.468 2xFp
78.67 5xFp
BTSC Baseband Frequency (KHz)

Fig. 1

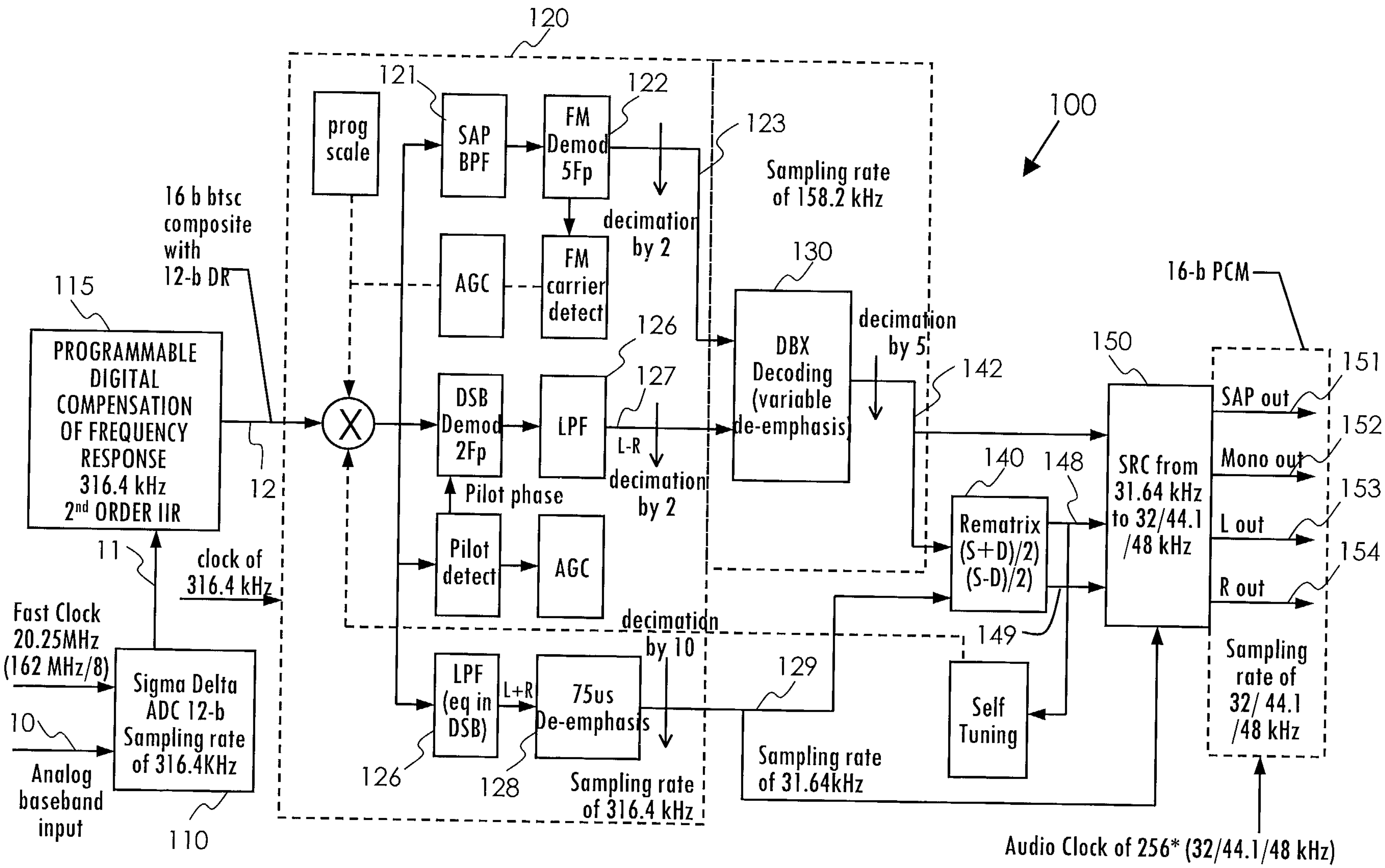
100
PROGRAMMABLE DIGITAL COMPENSATION OF FREQUENCY RESPONSE 316.4 kHz 2nd ORDER IIR
115
16 b btsc composite with 12-b DR
12
11
clock of 316.4 kHz
Fast Clock 20.25MHz (162 MHz/8)
10
Analog baseband input
Sigma Delta ADC 12-b Sampling rate of 316.4KHz
110
120
prog scale
121
SAP BPF
122
FM Demod 5Fp
decimation by 2
AGC
FM carrier detect
DSB Demod 2Fp
Pilot phase
Pilot detect
AGC
126
LPF
127
L-R
decimation by 2
LPF (eq in DSB)
L+R
126
75us De-emphasis
128
decimation by 10
Sampling rate of 316.4 kHz
123
Sampling rate of 158.2 kHz
130
DBX Decoding (variable de-emphasis)
decimation by 5
142
129
Sampling rate of 31.64kHz
140
Rematrix (S+D)/2) (S-D)/2)
148
149
Self Tuning
150
SRC from 31.64 kHz to 32/44.1 /48 kHz
16-b PCM
SAP out
Mono out
L out
R out
151
152
153
154
Sampling rate of 32/ 44.1 /48 kHz
Audio Clock of 256* (32/44.1/48 kHz)

Fig. 2

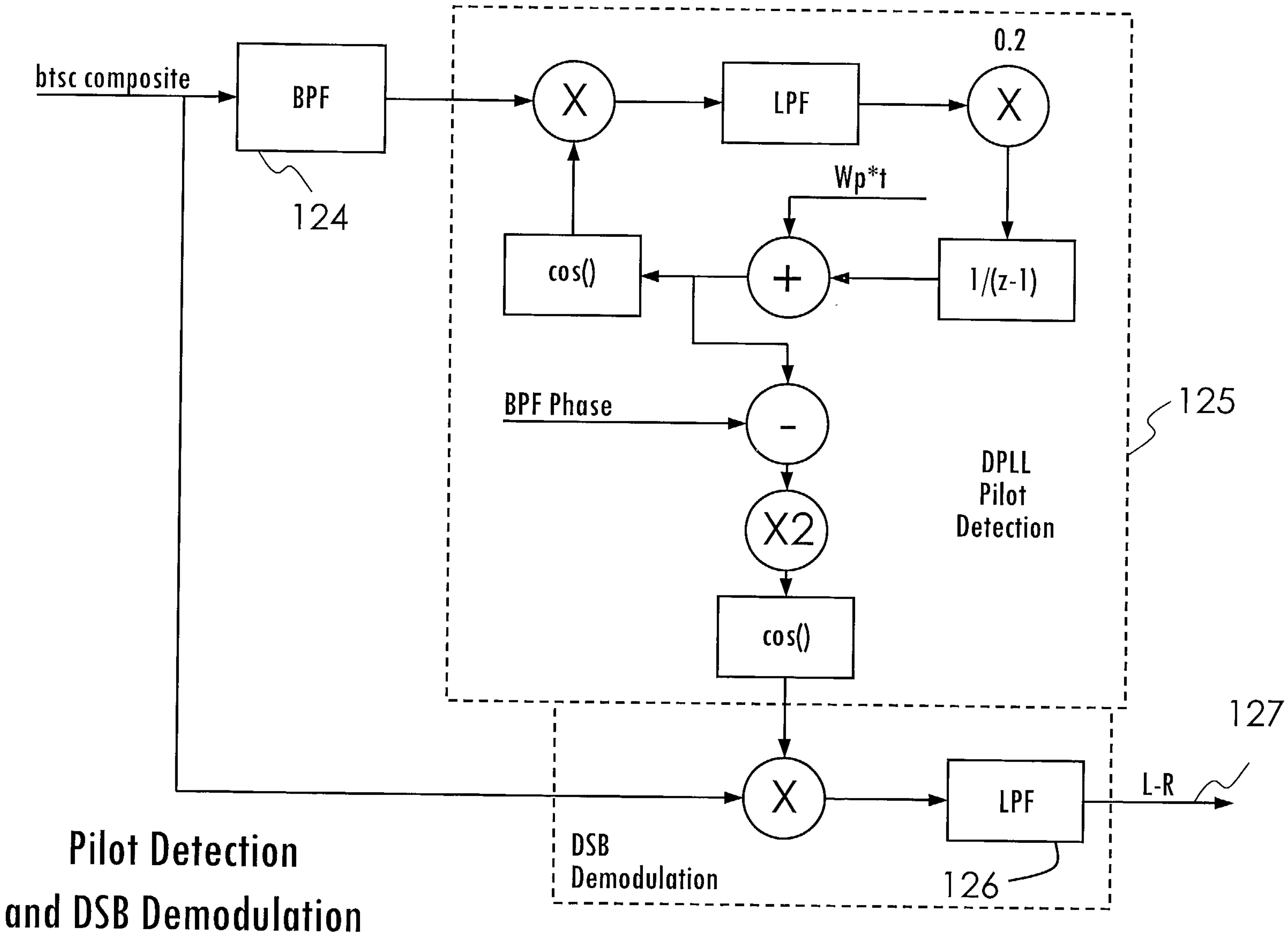
btsc composite
BPF
124
X
LPF
0.2
X
Wp*t
cos()
+
1/(z-1)
BPF Phase
-
X2
cos()
125
DPLL
Pilot
Detection
127
X
LPF
L-R
DSB
Demodulation
126
Pilot Detection
and DSB Demodulation

Fig. 2B

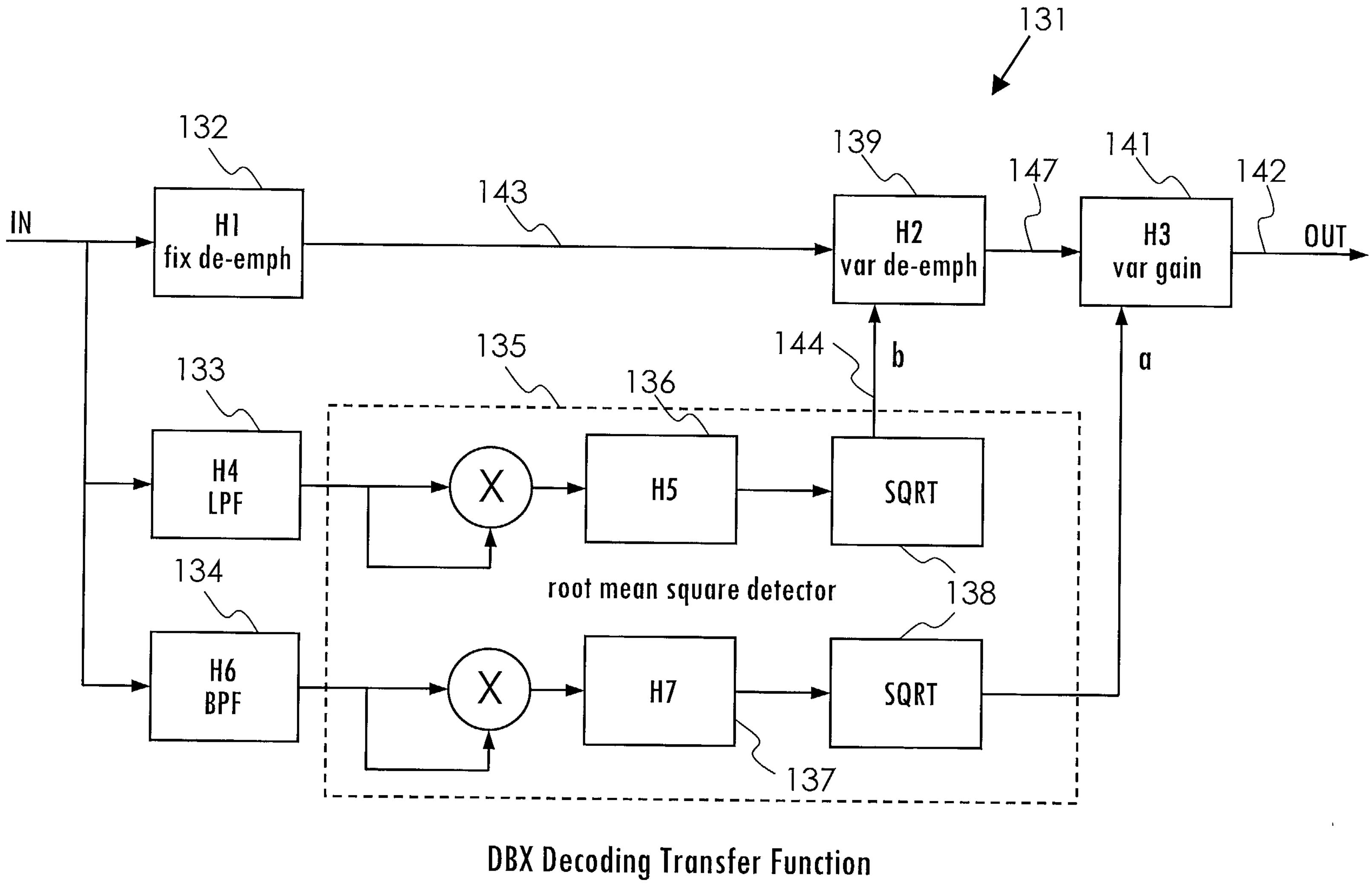
131
IN
H1
fix de-emph
132
143
H2
var de-emph
139
147
H3
var gain
141
142
OUT
H4
LPF
133
H6
BPF
134
135
X
H5
136
SQRT
144
b
a
root mean square detector
138
X
H7
SQRT
137
DBX Decoding Transfer Function

Fig. 3

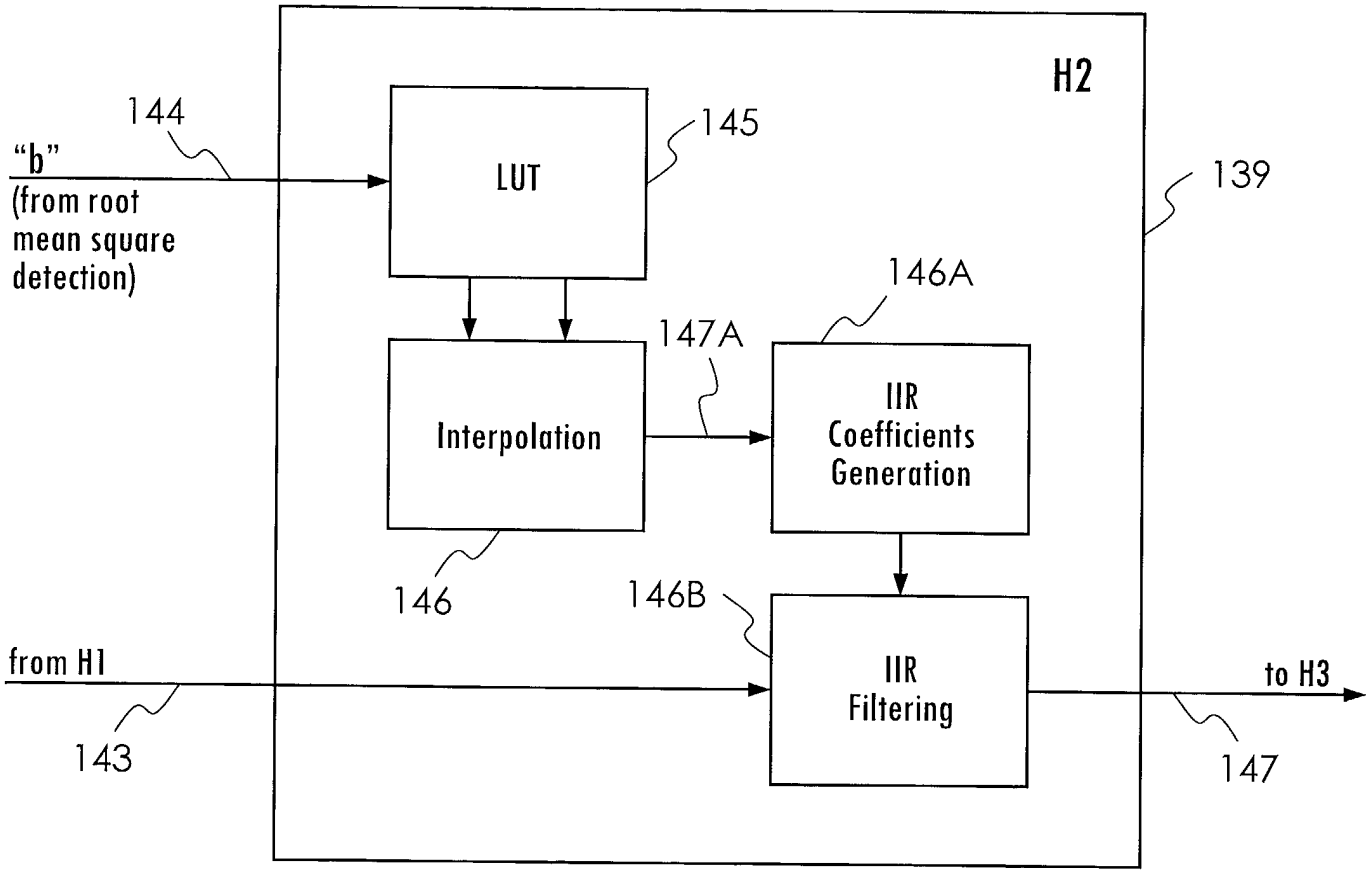
H2
144
"b"
(from root
mean square
detection)
LUT
145
139
146A
147A
Interpolation
IIR
Coefficients
Generation
146
146B
from H1
IIR
Filtering
to H3
143
147

Fig. 3B

160

$$H1(s) = \frac{\frac{s}{5.23 \times 2\pi} + 1}{\frac{s}{0.408 \times 2\pi} + 1} \times \frac{\frac{s}{62.5 \times 2\pi} + 1}{\frac{s}{2.19 \times 2\pi} + 1}$$

$$H2(s) = \frac{1 + \left(\frac{s}{20.1 \times 2\pi}\right)\left(\frac{b + 51b}{b + 1}\right)}{1 + \left(\frac{s}{20.1 \times 2\pi}\right)\left(\frac{1 + 51}{b + 1}\right)}$$

$$H3(s) = a$$

$$H4(s) = \frac{\left(\frac{s}{7.66 \times 2\pi}\right)^2}{\left[\left(\frac{s}{7.66 \times 2\pi}\right)^2 + \left(\frac{s}{7.31 \times 2\pi}\right) + 1\right]} \times \frac{1}{\left[\left(\frac{s}{26.9 \times 2\pi}\right) + 1\right]} \times \frac{\left(\frac{s}{3.92 \times 2\pi}\right)}{\left[\left(\frac{s}{3.92 \times 2\pi}\right) + 1\right]}$$

$$H5(s) = \frac{a2}{s + a2}$$

$$H6(s) = \frac{\left(\frac{s}{0.0354 \times 2\pi}\right)}{\left(\frac{s}{0.0354 \times 2\pi} + 1\right)\left(\frac{s}{2.09 \times 2\pi} + 1\right)}$$

$$H7(s) = \frac{a1}{s + a1}$$

165

165A

$$H1(z) = \frac{(0.0857 - 0.0696z^{-1})(0.0909 - 0.0076z^{-1})}{(1.0 - 0.9839z^{-1})(1.0 - 0.9167z^{-1})}$$

$$H2(z) = \frac{(103*b+3) - z^{-1}(101*b+1)}{(3*b+3) - z^{-1}(b+101)}$$

$$H3(z) = a$$

$$H4(z) = \frac{0.5715 * 0.45085 * (1 - z^{-1})^3}{(1.0 - 2.0 * 0.5997\, z^{-1} + 2.0 * 0.1470\, z^{-2})(1.0 - 2.0 * 0.8242\, z^{-1} + 2.0 * 0.3635\, z^{-2})}$$

$$H5(z) = \frac{0.047^2}{1 - 0.99945\, z^{-1}}$$

$$H6(z) = \frac{0.07959\,(1 - z^{-2})}{1 - 2.0 * 0.9595\, z^{-1} + 2.0 * 0.4595\, z^{-2}}$$

$$H7(z) = \frac{0.02699^2}{1 - 0.9998\, z^{-1}}$$

The square root calculation is done through the following equation

$$y[0] = 0.66667 * sq\_in + 0.354167$$

$$sqrt = coef12 * (sq\_in - y[0] * y[0]) + y[0]$$

The value of sq_in is between 1.0 to 0.25, and coef12 is one of 12 coefficients chosen based on sq_in.

Fig. 4

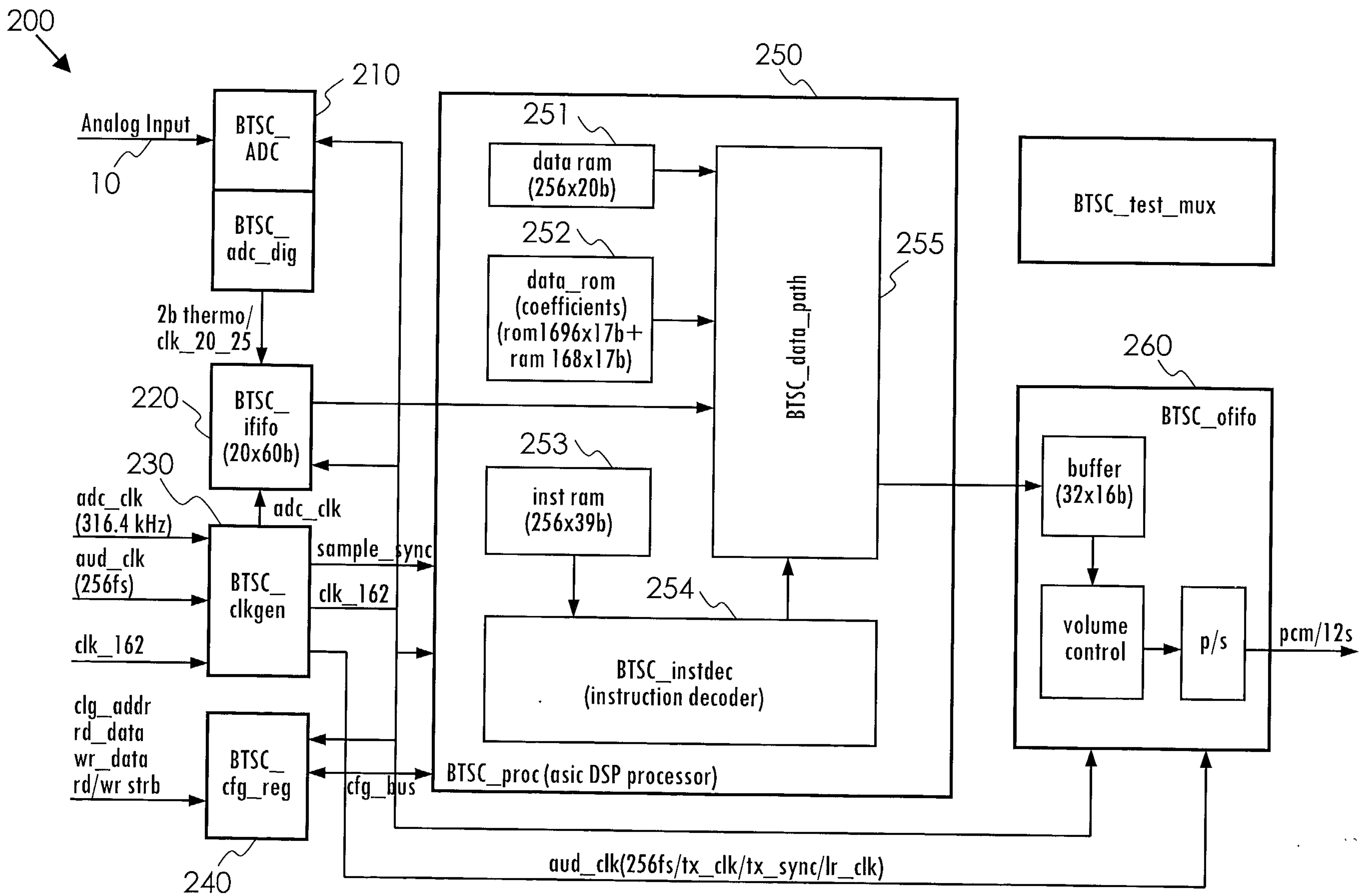
200
Analog Input
10
BTSC_ ADC
210
BTSC_ adc_dig
2b thermo/ clk_20_25
BTSC_ ififo (20x60b)
220
adc_clk
230
adc_clk (316.4 kHz)
aud_clk (256fs)
clk_162
BTSC_ clkgen
sample_sync
clk_162
clg_addr
rd_data
wr_data
rd/wr strb
BTSC_ cfg_reg
240
cfg_bus
250
251
data ram (256x20b)
252
data_rom (coefficients) (rom1696x17b+ ram 168x17b)
253
inst ram (256x39b)
254
BTSC_instdec (instruction decoder)
255
BTSC_data_path
BTSC_proc (asic DSP processor)
BTSC_test_mux
260
BTSC_ofifo
buffer (32x16b)
volume control
p/s
pcm/12s
aud_clk(256fs/tx_clk/tx_sync/lr_clk)

Fig. 5

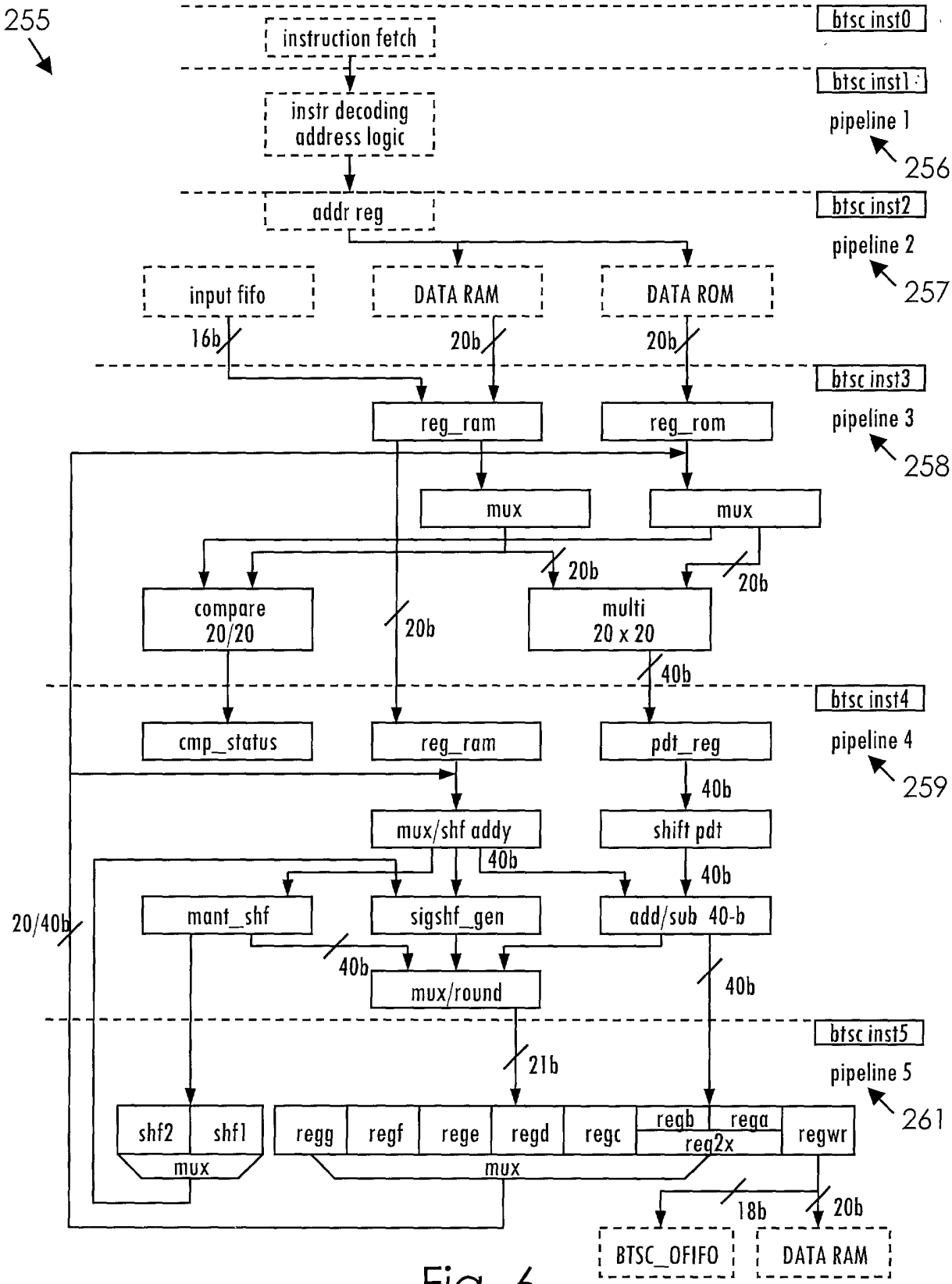
255
instruction fetch
instr decoding address logic
addr reg
input fifo
DATA RAM
DATA ROM
16b
20b
20b
reg_ram
reg_rom
mux
mux
20b
20b
compare 20/20
20b
multi 20 x 20
40b
cmp_status
reg_ram
pdt_reg
40b
mux/shf addy
shift pdt
40b
40b
20/40b
mant_shf
sigshf_gen
add/sub 40-b
40b
mux/round
40b
21b
shf2
shf1
mux
regg
regf
rege
regd
regc
regb
rega
reg2x
regwr
mux
18b
20b
BTSC_OFIFO
DATA RAM
btsc inst0
btsc inst1
pipeline 1
256
btsc inst2
pipeline 2
257
btsc inst3
pipeline 3
258
btsc inst4
pipeline 4
259
btsc inst5
pipeline 5
261

Fig. 6

300

CODE	INSTRUCTION	CYCLES	DESCRIPTION
0	nop	1	no operation
1	mant	1	mantissa and exponent generation from 40-b register
2	sigshf	1	convert from mantissa and exponent to fixed-point signal
3	mults	1	multiplication and subtraction
4	multa	1	multiplication and add
5	fos	3	micro code do 20-b 1st order IIR filter which is made of 3 mults/multa
6	sos	5	micro code does 20-b 2nd order IIR filter which is made of 5 mults/multa
7	rms	6	micro code does 20-b square and 40-b 1st order IIR filter. which is consisted of 6 mults/multa
8	halt	1	halt programe
9	setli	1	setup inner loop
10	setlo	1	setup outer loop
11	jmpif	1	conditional jump
12	call	1	call routine
13	cmp	1	compare two register value and store 1-b result in status register
14	fos2	6	micro code does 40-b 1s order IIR filter, which is consisted of 6 mults/multa
15	dload	1	directly store coded data to register ram location

301, 302

Fig. 7